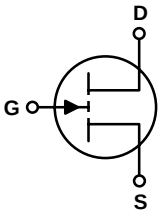
INN100W135A-Q

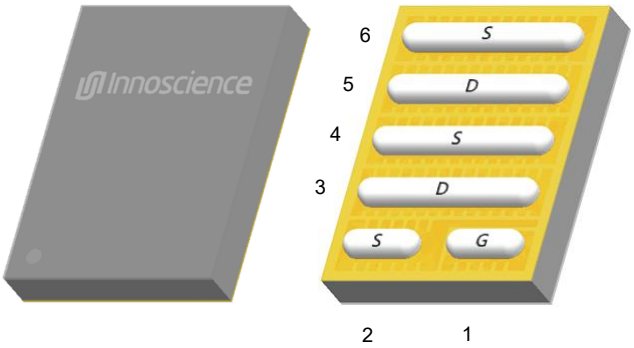
1. General description

GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in WLCSP with 2.13 mm x 1.63 mm package size.



2. Features

- AEC-Q101 Qualified
- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Very small package size
- Zero reverse recovery charge



Top View Bottom View

3. Applications

- LiDAR Application
- High Power Density DC-DC Converters
- Class-D Audio
- High Intensity Headlamps

4. Key performance parameters

Table 1 Key performance parameters at T_J = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	100	V
$R_{DS(on),max}$ @ V_{GS} = 5 V	13.5	mΩ
$Q_{G,typ}$ @ V_{DS} = 50V	3.2	nC
$I_{DS,Pulse}$(T_A = 25 °C)	75	A
Q_{OSS}@ V_{DS} = 50V	20	nC

5. Pin information

Table 2 Pin information

PIN	Pin Description	Pin Function
1	Gate	Driver Gate
3,5	Drain	Power Drain
2,4,6	Source	Power Source

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN100W135A-Q	WLCSP 2.13x1.63	J24

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6. Maximum ratings

at T_J = 25 °C unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
I_D	Continuous current (T_A = 25 °C)	18	A
	Pulsed (T_A = 25 ˚C, T_{PULSE} = 300 μs)	75	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-55 to 150	˚C

7. Thermal characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
$R_{\theta JC}$	Thermal Resistance, Junction to Case	15.62	˚C/W	-
$R_{\theta JB}$	Thermal Resistance, Junction to Board	2.80	˚C/W	-
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient [1]	66.29	˚C/W	-
T_{sold}	Maximum reflow soldering temperature	260	°C	MSL1

Note:

1. $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad，single layer 2 oz copper on FR4 board.

8. Electric characteristics

at T_J = 25 °C unless otherwise specified.

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Voltage	100	-	-	V	V_{GS} = 0 V, I_D = 550 µA
I_{DSS}	Drain Source Leakage	-	1	100	µA	V_{GS} = 0 V, V_{DS} =100 V
I_{GSS}	Gate-to-Source Forward Leakage (25°C)	-	3	100	µA	V_{GS} = 6 V, VDS = 0V
	Gate-to-Source Reverse Leakage	-	0.1	10	µA	V_{GS} = -4 V, VDS = 0V
$V_{GS(TH)}$	Gate Threshold Voltage	0.7	1.1	2.5	V	V_{DS} = V_{GS}, I_D = 3 mA
$R_{DS(on)}$	Drain-Source On-state Resistance[2]	-	10	13.5	mΩ	V_{GS} = 5 V, I_D = 11 A
V_{SD}	Source-Drain Forward Voltage	-	1.6	-	V	I_{SD} = 0.5 A, V_{GS} = 0 V

Note:

2. $R_{DS(on)}$ is measured without prior drain bias or switching stress.

Table 7 Dynamic characteristics[3]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{ISS}	Input Capacitance	-	380	-	pF	V_{GS} = 0 V, V_{DS} = 50 V
C_{OSS}	Output Capacitance	-	200	-		V_{GS} = 0 V, V_{DS} = 50 V
C_{RSS}	Reverse Transfer Capacitance	-	2.1	-		V_{GS} = 0 V, V_{DS} = 50 V
$C_{OSS(ER)}$	Energy Related C_{OSS}	-	292	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V
$C_{OSS(TR)}$	Time Related C_{OSS}	-	400	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V
R_G	Gate resistance	-	1.5	-	Ω	f = 5MHz, open drain
Q_G	Total Gate Charge	-	3.2	-	nC	V_{GS} = 5 V, V_{DS} = 50 V, I_D= 11 A
Q_{GS}	Gate to Source Charge	-	0.7	-		V_{DS} = 50 V, I_D = 11 A
Q_{GD}	Gate to Drain Charge	-	0.5	-		V_{DS} = 50 V, I_D = 11 A
$Q_{G(TH)}$	Gate Charge at Threshold	-	0.5	-		V_{DS} = 50 V, I_D = 11 A
Q_{OSS}	Output Charge	-	20	-		V_{GS} = 0 V, V_{DS} = 50 V

Note:

3. Guaranteed by design.

9. Electric characteristics diagrams

at T_J = 25 °C unless otherwise specified.

Fig. 1 Typical Output Characteristics (T_J=25°C)

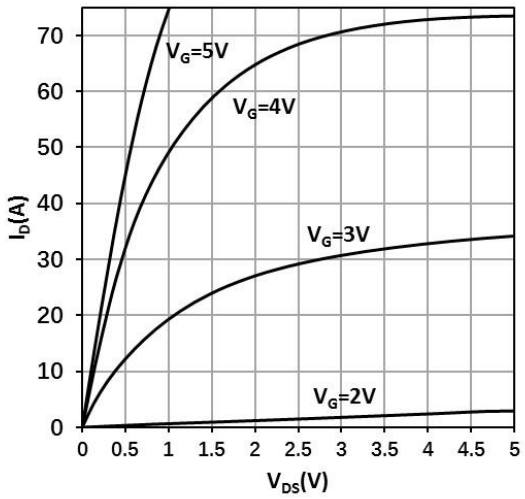


Fig. 2 Typical Output Characteristics (T_J=125°C)

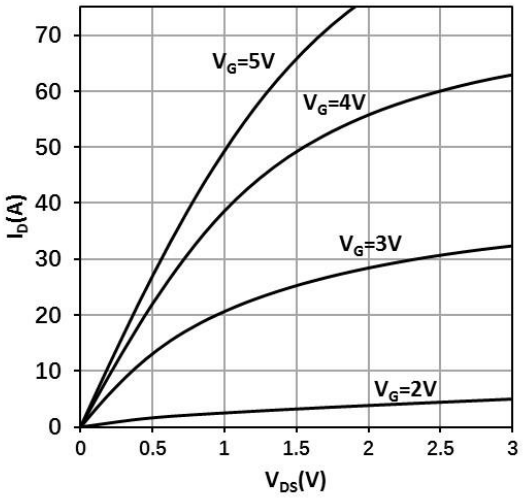


Fig. 3 Typical Drain On-state Resistance (T_J=25°C)

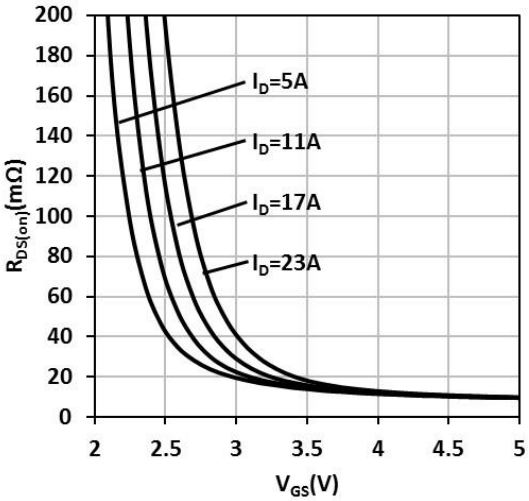


Fig. 4 Typical Drain On-state Resistance (T_J=125°C)

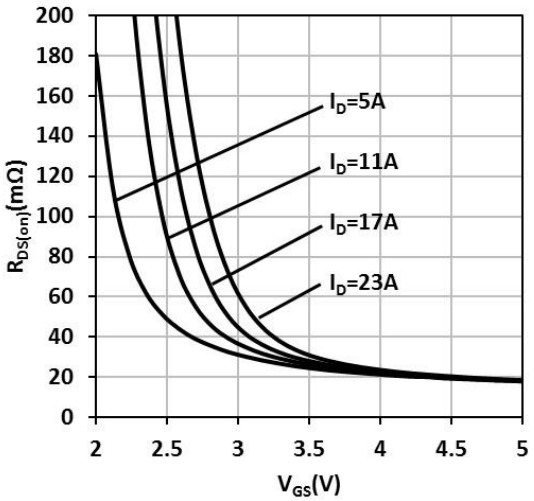


Fig. 5 Normalized On-State Resistance vs. Temp.

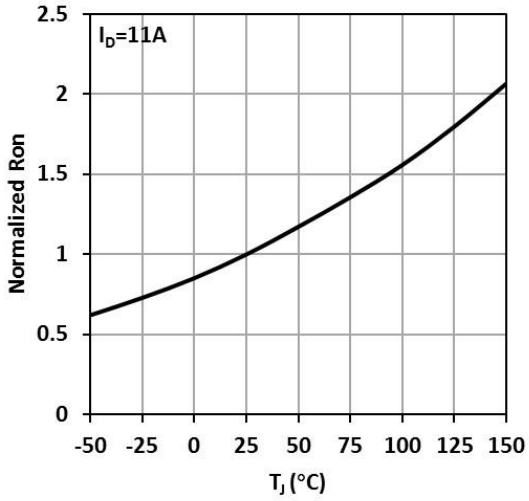


Fig. 6 Typical Transfer Characteristics

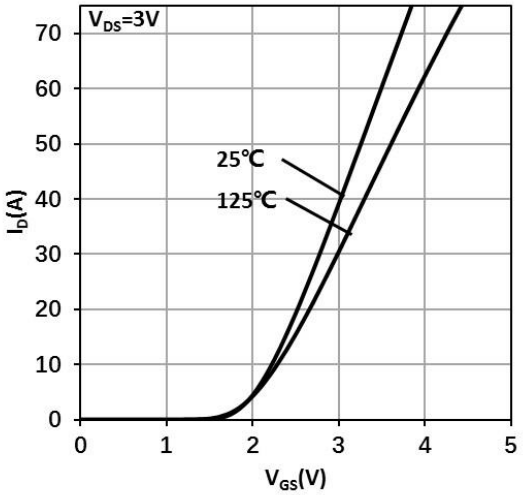


Fig. 7 Typ. Reverse Drain-Source Characteristics ($V_{GS}\leqslant 0, T_J$=25°C)

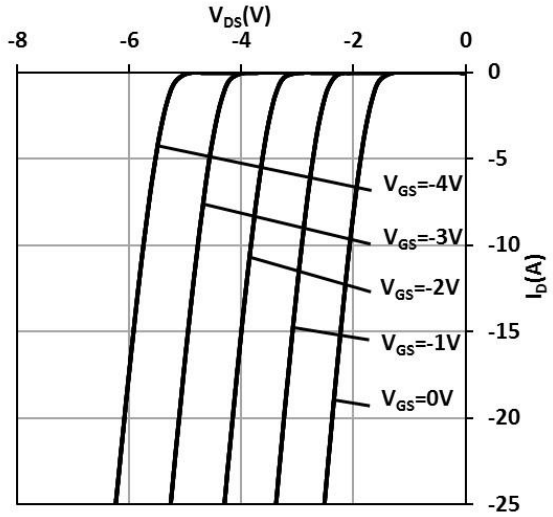


Fig. 8 Typ. Reverse Drain-Source Characteristics ($V_{GS}\geqslant 0, T_J$=25°C)

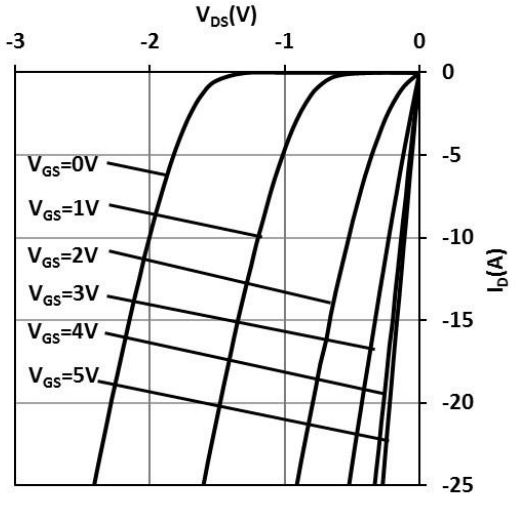


Fig. 9 Typ. Reverse Drain-Source Characteristics ($V_{GS}\leqslant 0$, T_J=125°C)

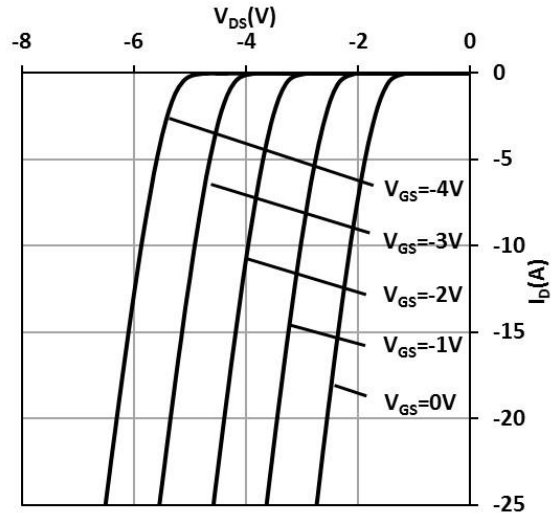


Fig. 10 Typ. Reverse Drain-Source Characteristics ($V_{GS}\geqslant 0$, T_J=125°C)

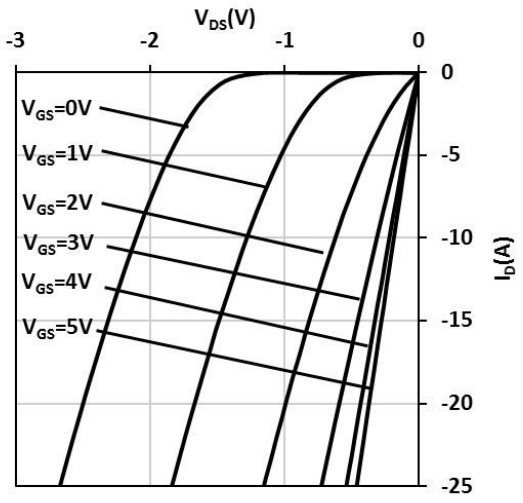


Fig. 11 Typ. Capacitances Characteristics

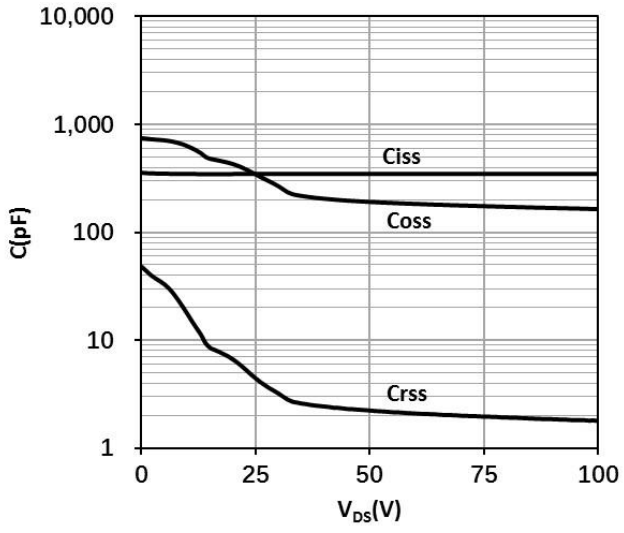


Fig. 12 Typ. Gate Charge

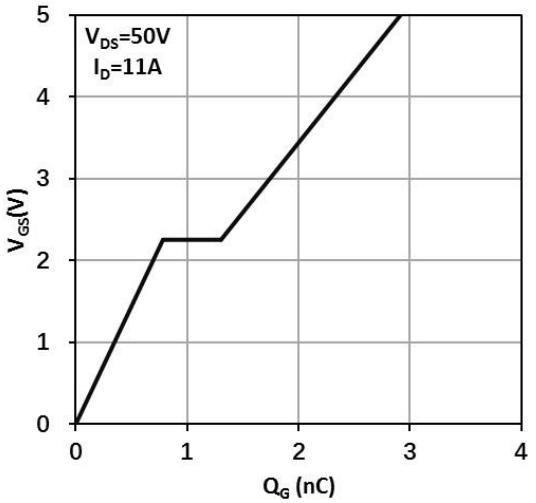


Fig. 13 Normalized Threshold Voltage vs. Temp.

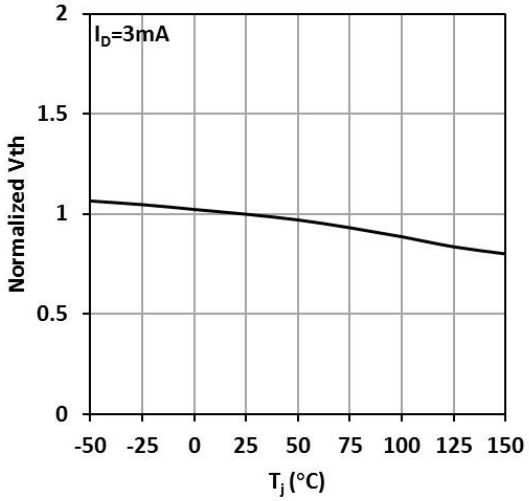


Fig. 14 Output Charge

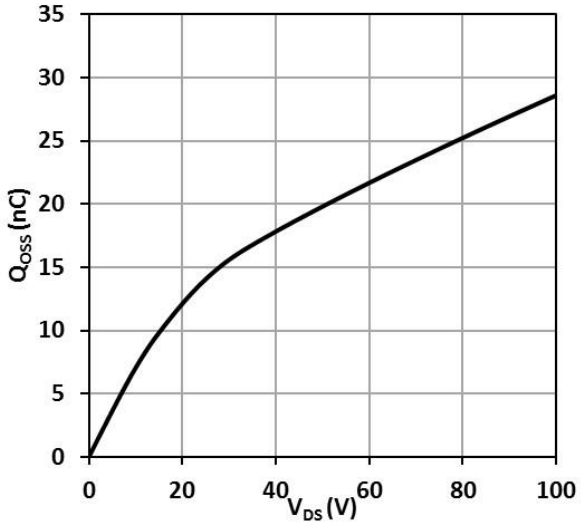


Fig. 15 Output Capacitance Stored Energy

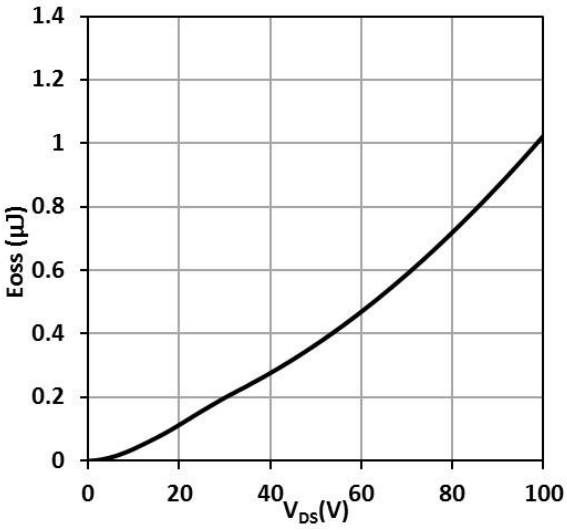


Fig. 16 Power Dissipation

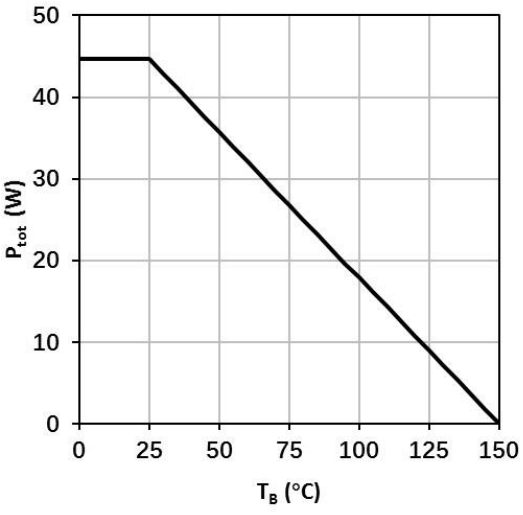


Fig. 17 Safe Operating Area

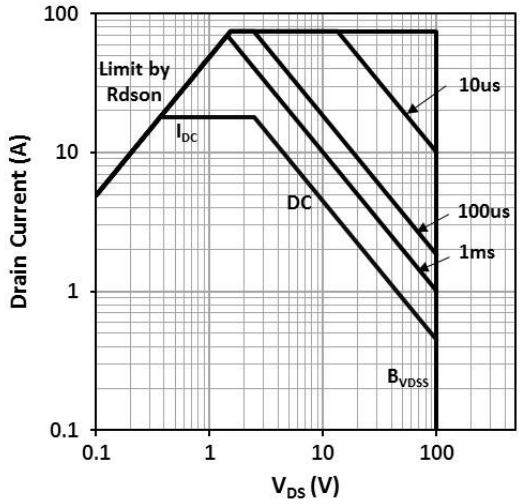
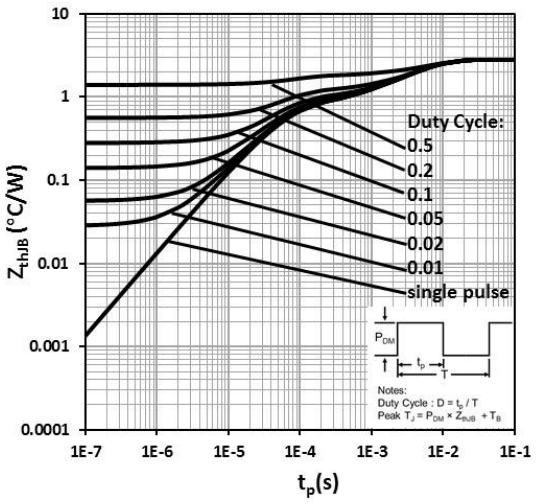
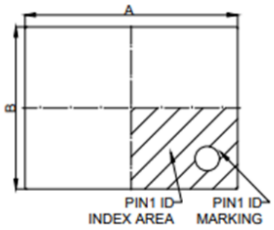


Fig. 18 Max. Transient Thermal Impedance

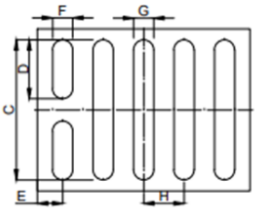


10. Package outlines

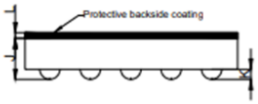
Package Reference



TOP VIEW



BOTTOM VIEW

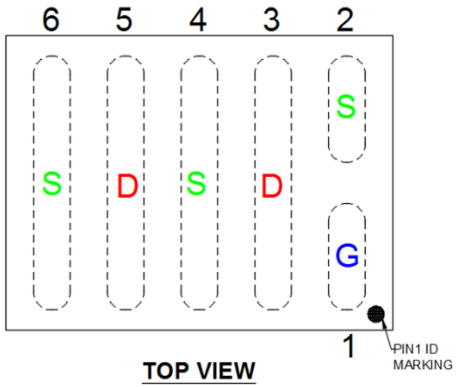


SIDE VIEW

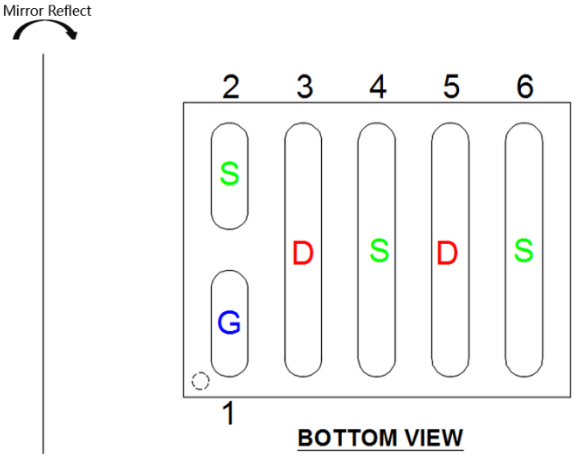
SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	2.105	2.130	2.155	
B	1.605	1.630	1.655	
C	1.362	1.382	1.402	4X
D	0.560	0.580	0.600	2X
E	0.265 REF			
F	0.180	0.200	0.220	2X
G	0.180	0.200	0.220	4X
H	0.4 BASIC			5X
J	0.374	0.409	0.444	
K	0.080	0.100	0.120	
L	0.022	0.025	0.028	

NOTE:
1)ALL DIMENSION ARE IN MILLIMETERS.
2)BOTTOM VIEW IS SOLDER BAR SIDE VIEW
3)BAR COPLANARITY SHALL BE 0.05 MILLIMETERS MAX.
4)COMPLIES WITH JEDEC MO-211.
5)DRAWING IS NOT TO SCALE.

PIN configuration

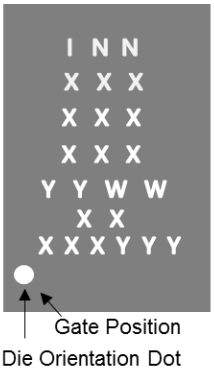


TOP VIEW



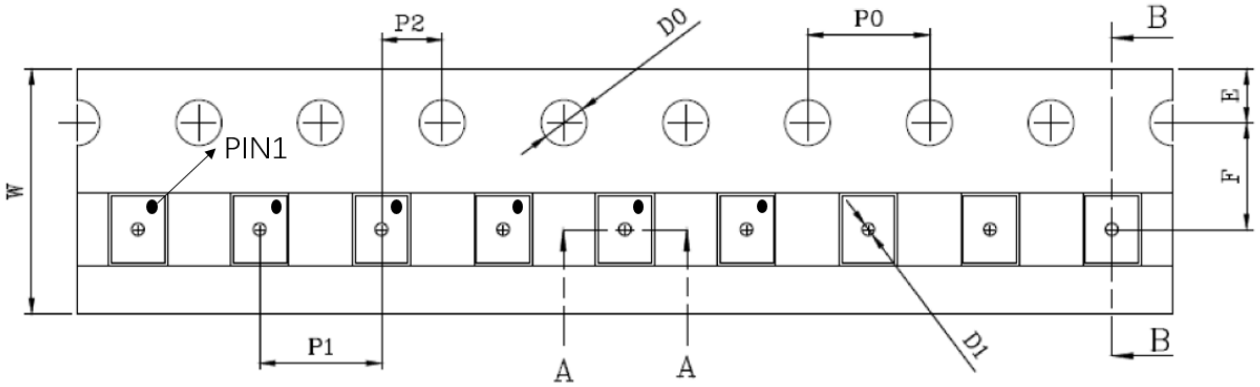
BOTTOM VIEW

Marking Reference:

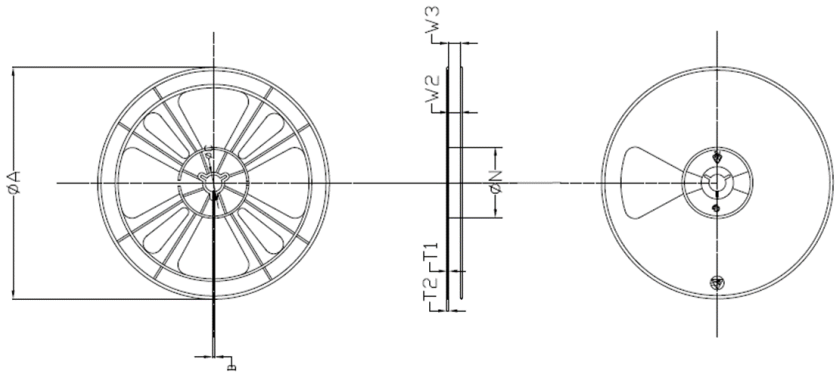


Row	Description	Example
Row 1	Company name	INN
Row 2	Product code	XXX
Row 3	Lot Code	XXX
Row 4		XXX
Row 5	Date code	YYWW
Row 6	Wafer ID	XX
Row 7	Location ID	XXXYYY

11. Reel information



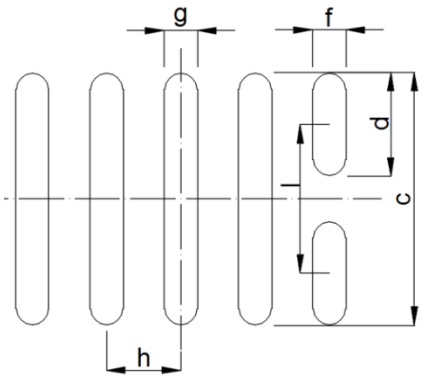
Item	Value&Tolerance(mm)
D0	1.5+0.10/-0.00
D1	0.40 ± 0.05
P0	4.00 ± 0.10
P1	4.00 ± 0.10
P2	2.00 ± 0.05
E	1.75 ± 0.10
F	3.50 ± 0.05
W	8.00+0.30/-0.10



Item	Value & Tolerance (mm)
A	179±1.0
B	2.0±0.2
C	13.5±0.2
N	54.8±0.2
W2	9.0±0.2
W3	9.2±1.0
T1	1.2±0.2
T2	1.5±0.2

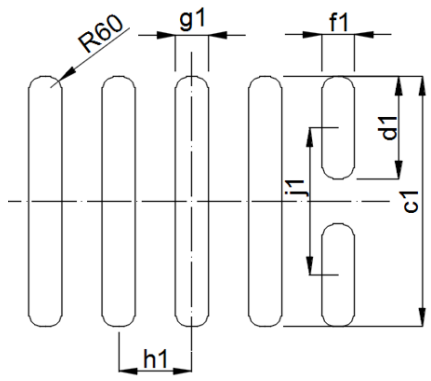
12. Land Pattern

Recommended land pattern



SYMBOL	MILLIMETER	NOTE
	NOM	
c	1.362	4x
d	0.560	2x
f	0.180	2x
g	0.180	4x
h	0.400	5x
l	0.802	

Recommended Stencil drawing



SYMBOL	MILLIMETER	NOTE
	NOM	
c1	1.362	4x
d1	0.560	2x
f1	0.180	2x
g1	0.180	4x
h1	0.400	5x
j1	0.802	

13. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2023-11-27	Version 1.0 Release
1.01	2024-12-09	1. Delete error unit annotation in Land pattern; 2. Add I_D Pulse test condition in Table 1, I_D Continuous test condition in Table 4 and Add Note in Table 6,7; 3. Add test condition I_D = 3mA in Fig.13; 4. Add Pin1 mark in Reel information.

Important Notice

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